PL520-20

Low Phase Noise VCXO (for 100-200MHz Fundamental Crystals)

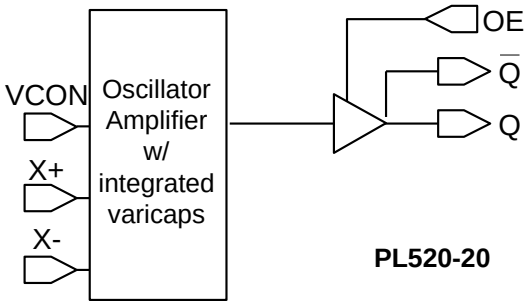
FEATURES

- 100MHz to 200MHz Fundamental Mode Crystals
- Output range (no PLL):
  - 100MHz – 200MHz (3.3V).
  - 100MHz – 170MHz (2.5V).
- Low Injection Power for crystal 50uW.
- Complementary outputs: CMOS, PECL or LVDS.
- Selectable OE Logic (enable high or enable low).
- Integrated variable capacitors.
- Supports 2.5V or 3.3V-Power Supply.
- Available in die form.
- Die thickness is 10 mil.

DESCRIPTION

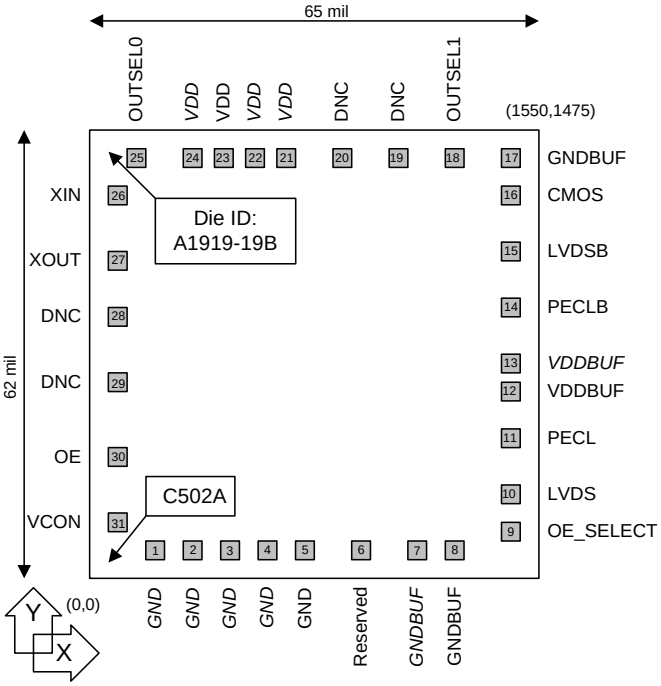
PL520-20 is a VCXO IC specifically designed to pull high frequency fundamental crystals. Its design was optimized to tolerate higher limits of inter-electrode capacitance and bonding capacitance to improve yield. It achieves very low current into the crystal resulting in better overall stability. Its internal varicaps allow on-chip frequency pulling, controlled by the VCON input.

BLOCK DIAGRAM



PL520-20

DIE CONFIGURATION



DIE SPECIFICATIONS

Name	Value
Size	62 x 65 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	10 mil

OUTPUT SELECTION AND ENABLE

Pad #18 OUTSEL1	Pad #25 OUTSEL0	Selected Output
0	0	High Drive CMOS
0	1	Standard CMOS
1	0	LVDS
1	1	PECL (default)

OE_SELECT (Pad #9)	OE (Pad #30)	State
0	0	Tri-state
	1 (Default)	Output enabled
1 (Default)	0 (Default)	Output enabled
	1	Tri-state

Pad #9, 18, 25: Bond to GND to set to "0", bond to VDD to set to "1"
No connection results to "default" setting through internal pull-up/-down.
Pad #30: Logical states defined by PECL levels if OE_SELECT (pad #9) is "1"
Logical states defined by CMOS levels if OE_SELECT is "0"

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ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature for 3.3V Supplies	T_A	-40	85	°C
Ambient Operating Temperature for 2.5V Supplies	T_A	-20	70	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	Parallel Fundamental Mode 3.3V Supplies 2.5V Supplies	 100 100		 200 170	MHz
Crystal Loading Rating	$C_{L\ (xtal)}$	3.3V Supply Die at VCON = 1.65V		4		pF
		2.5V Supply Die at VCON = 1.25V		5		pF
Interelectrode Capacitance	C_0				3.5	pF
Crystal Pullability	$C_0/C_{1\ (xtal)}$	AT cut			250	-
Recommended ESR	R_E	AT cut 3.3V Supplies 2.5V Supplies			 30 15	Ω

3. Voltage Control Crystal Oscillator

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid		10		ms
VCXO Tuning Range *		XTAL C_0/C_1 < 250 3.3V Supplies 2.5V Supplies	 180 145			ppm
VCXO Pullability *		0V ≤ VCON ≤ V_{DD} (at 25°C) 3.3V Supplies 2.5V Supplies		 ±100 ±80		ppm
On-chip Varicaps Control Range *		VCON = 0 to V_{DD} 3.3V Supplies 2.5V Supplies		 5 – 15 6 – 15		pF
Linearity *		3.3V Supplies 2.5V Supplies		4 5	5 10	%
VCXO Tuning Characteristic				65		ppm/V
VCON Input Impedance				60		kΩ
VCON Modulation BW		0V ≤ VCON ≤ V_{DD}, -3dB	25			kHz

Note: Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits.

4. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (Loaded Outputs)	I_{DD}	PECL/LVDS/CMOS			70/40/40	mA
Operating Voltage	V_{DD}	3.3V Supplies 2.5V Supplies	3.13 2.375		3.47 2.625	V
Output Clock Duty Cycle		@ 1.25V (LVDS), 3.3V Supply @ V_{DD} – 1.3V (PECL), 3.3V Supply	45 45	50 50	55 55	%
		@ 1.25V (LVDS), 2.5V Supply @ V_{DD} – 1.3V (PECL), 2.5V Supply	43 43	50 50	57 57	%
Short Circuit Current				±50		mA

5. Jitter Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period Jitter RMS at 155MHz *	At 155.52MHz, with capacitive decoupling between VDD and GND. Over 10,000 cycles		2.5		ps
Period Jitter peak-to-peak at 155MHz *			18.5	20	
Accumulated Jitter RMS at 155MHz *	At 155.52MHz, with capacitive decoupling between VDD and GND. Over 1,000,000 cycles.		2.5		ps
Accumulated Jitter peak-to-peak, 155MHz *			24	27	
Random Jitter *			2.5		ps
Integrated jitter RMS at 155MHz	Integrated 12 kHz to 20 MHz		0.3	0.4	ps

* Measured on Wavecrest SIA 3000 at VDD=3.3V

6. Phase Noise Specifications

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	UNITS
Phase Noise relative to carrier	155.52MHz	-75	-95	-125	-140	-145	dBc/Hz

Note: Phase Noise measured at VCON = 0V, VDD=3.3V

7. CMOS Electrical Specifications

3.3V Supplies

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output drive current (High Drive)	I_{OH}	V_{OH}= V_{DD}-0.4V, V_{DD}=3.3V	30			mA
	I_{OL}	V_{OL} = 0.4V, V_{DD} = 3.3V	30			mA
Output drive current (Standard Drive)	I_{OH}	V_{OH}= V_{DD}-0.4V, V_{DD}=3.3V	10			mA
	I_{OL}	V_{OL} = 0.4V, V_{DD} = 3.3V	10			mA
Output Clock Rise/Fall Time (Standard Drive)		0.3V ~ 3.0V with 15 pF load		2.4		ns
Output Clock Rise/Fall Time (High Drive)		0.3V ~ 3.0V with 15 pF load		1.2		

2.5V Supplies

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output drive current (High Drive)	I_{OH}	V_{OH}= V_{DD}-0.4V, V_{DD}=3.3V	20			mA
	I_{OL}	V_{OL} = 0.4V, V_{DD} = 3.3V	20			mA
Output drive current (Standard Drive)	I_{OH}	V_{OH}= V_{DD}-0.4V, V_{DD}=3.3V	6.5			mA
	I_{OL}	V_{OL} = 0.4V, V_{DD} = 3.3V	6.5			mA
Output Clock Rise/Fall Time (Standard Drive)		0.25V ~ 2.25V with 15 pF load		3.0		ns
Output Clock Rise/Fall Time (High Drive)		0.25V ~ 2.25V with 15 pF load		1.5		

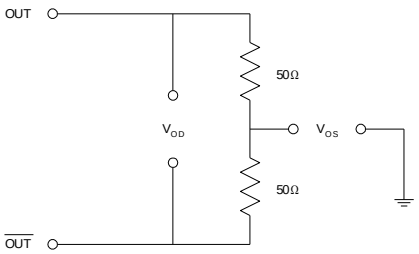
8. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V_{OD}	R_L = 100 Ω (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	V_{out} = V_{DD} or GND, V_{DD} = 0V		±1	±10	uA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

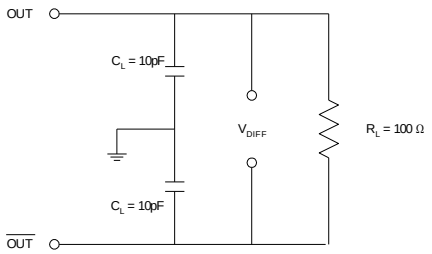
9. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	t_r	R_L = 100 Ω, C_L = 10 pF (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns

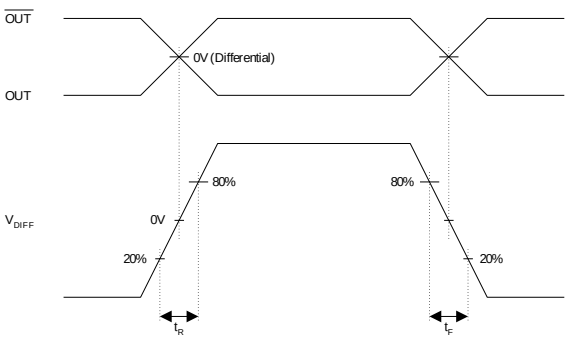
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transistion Time Waveform



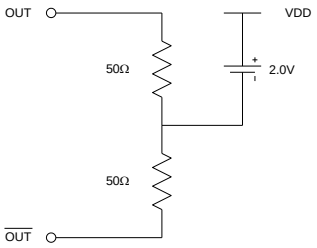
10. PECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	V_{OH}	R_L = 50 Ω to (V_{DD} – 2V) (see figure)	V_{DD} – 1.025		V
Output Low Voltage	V_{OL}			V_{DD} – 1.620	V

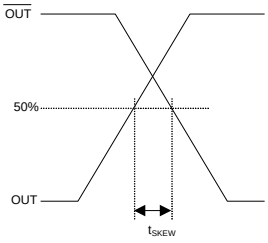
11. PECL Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	t_r	@20/80% - PECL		0.6	1.5	ns
Clock Fall Time	t_f	@80/20% - PECL		0.5	1.5	ns

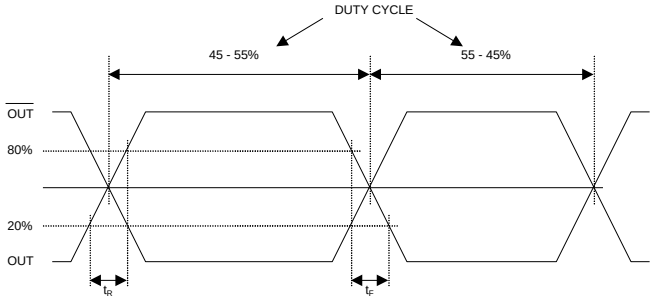
PECL Levels Test Circuit



PECL Output Skew



PECL Transistion Time Waveform



PAD ASSIGNMENT

Pad #	Name	X (µm)	Y (µm)
1	GND	248	109
2	GND	361	109
3	GND	473	109
4	GND	587	109
5	GND	702	109
6	DNC (Do Not Connect)	874	109
7	GND	1042	109
8	GNDBUF	1171	109
9	OE_SELECT	1400	125
10	LVDS	1400	259
11	PECL	1400	476
12	VDDBUF	1400	616
13	VDDBUF	1400	716
14	PECLB	1400	871
15	LVDSB	1400	1089
16	CMOS	1400	1227
17	GNDBUF	1389	1365
18	OUTSEL1	1232	1365
19	DNC (Do Not Connect)	1042	1365
20	DNC (Do Not Connect)	854	1365
21	VDD	659	1365
22	VDD	559	1365
23	VDD	459	1365
24	VDD	358	1365
25	OUTSEL0	194	1365
26	XIN	109	1223
27	XOUT	109	1017
28	DNC (Do Not Connect)	109	858
29	DNC (Do Not Connect)	109	646
30	OE	109	397
31	VCON	109	181

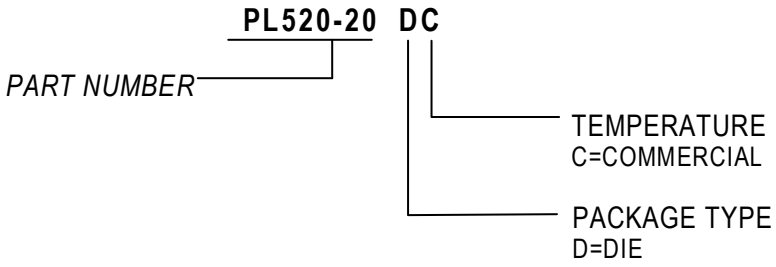
Note: for optimal Phase Noise performance, it is recommended to bond all optional VDD and GND pads.

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ORDERING INFORMATION

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range



Order Number	Marking	Package Option
PL520-20DC	PL520-20DC	Die – Waffle Pack

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